REMARKS

At the outset, the Examiner is thanked for the review and consideration of the pending application. The Non-Final Office Action dated May 1, 2008 has been received and reviewed. Reconsideration of the pending application is respectfully requested in view of the following observations.

1. Status of Pending Claims.

By this Response no claims are hereby amended. No claims are hereby cancelled. No claims are hereby newly added.

Claims 20-38 are thus pending.

2. Claim 31 is rejected under 35 U.S.C. §112(2) as indefinite.

The Examiner has rejected claim 31 as indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The rejection of claim 31 as indefinite is respectfully traversed.

In rejecting claim 31, the Examiner states, "the wording 'remains ... after standard CMOS process' is unclear, since it does not point out what a standard CMOS process is. Additionally, the claim fails to point out the method's steps which ensure the claimed behavior of the material such as "density of charge trap remains higher than or equal to $10^{11}/cm^2/eV$ (Office Action at page 2)."

In response to the Examiner's indefiniteness rejection, Applicant has conducted a word search on the term "standard CMOS" in granted claims of United States patents.

United States patent 7,376,040 B2 (*Matsumoto*) claims "said backup circuit includes devices which are capable of being formed by a standard CMOS process (Claim 1, Line 39)."

United States patent 4,165,642 (*Lipp*) claims "[t]he monolithic integrated circuit set forth in claim 1 formed in a standard CMOS chip fabrication process (Claim 2, Lines 5-7)" and "[t]he monolithic integrated circuit set forth in claim 2

formed in a standard metal gate CMOS chip fabrication process (Claim 3, Lines 8-10)."

At least *Lipp* was filed on March 22, 1978. Therefore, for at least 30 years, The United States Patent & Trademark Office has recognized the term "standard CMOS process" and thus it is respectfully submitted that one of ordinary skill in the art of manufacturing multilayer semiconductor structures would understand what is meant by the term "standard CMOS process."

Furthermore, upon careful reading of the Examiner's statement, "the claim fails to point out the method's steps which ensure the claimed behavior of the material", Applicant finds this to be unclear.

Claim 31 does not claim a behavior of a material. Rather, claim 31 claims a CMOS process that results in or contributes to a density of charge traps. Furthermore, claim 31 depends (indirectly) from claim 20 and thus necessarily contains all of the limitations from claim 20. Claim 20 is believed to be clear and definite.

Accordingly, withdrawal of the rejection of claim 31 as indefinite is respectfully requested.

3. Claims 20-24, 27-33 and 35-38 are rejected under 35 U.S.C. §103(a) as unpatentable over United States patent application publication 2003/0129780 A1 (*Auberton-Herve*) in view of Applicant's Admitted Prior Art (*AAPA*).

The rejection of claims 20-24 and 27-31 is respectfully traversed and reconsideration is requested.

Claims 20-24 and 27-31 are allowable over the combination of references in that each of these claims recite a combination of elements including, for example, "... a high resistivity silicon substrate with resistivity higher than 3 kΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer, wherein the method comprises suppressing ohmic losses inside the high resistivity silicon substrate by increasing charge trap density between the insulating layer and the silicon substrate." None of the cited references, singly or in combination, teach or suggest at least these features of the claimed invention.

Turning to *Auberton-Herve*, paragraph [0044] states that, "the layer of polycrystalline material can constitute a layer for trapping metallic impurities, which

is known to the skilled person as 'gettering' and is very beneficial in some applications."

"Gettering" by definition means the introduction of a material in small amounts during a chemical or metallurgical process to absorb impurities.

Gettering is not necessarily the same thing as charge trap density.

In fact, even if, *arguendo*, "gettering" could be thought of as equivalent to "charge trap density", there is still nothing in *Auberton-Herve* that teaches or suggests *increasing* (gettering) between the insulating layer and silicon substrate. Accordingly, the layer of *Auberton-Herve* is not present to remedy the reduction of substrate resistivity related to the presence of free carriers.

In the claimed invention, charge trap density is increased. This does not mean that impurities from other layers are trapped, as is the case of *Auberton-Herve*. Instead, in the claimed invention, free charges which appear at the interface between the insulating layer of the multilayer structure and the substrate are trapped such that *ohmic losses are reduced*.

Such charge traps play an important role in capturing free carriers, making them unable to react to high frequency electrical fields, meaning those fields having an operating frequency higher than 100 MHz. Thus, their contribution to high frequency ohmic losses is suppressed (Specification at page 16, lines 5-12).

An important charge trap density at the interface between the insulating layer and the substrate leads to the absorption of part of the electrons forming the superficial layer, which are gathered at the interface and which decrease the resistivity (and thus the electrical losses) of the multilayer structure. The higher the charge trap density, the more this effect, which thus decreases the losses. (Specification at page 18, lines 1-8).

Furthermore, the effect of the continuous voltage component which attracts near the interface negative (electrons) or positive (holes) charges, depending on the polarity of this voltage, is reduced by a more important charge trap density. A part of the mobile charges attracted towards the interface by the continuous voltage component are trapped so as to have no impact on high frequency losses (Specification at page 18, lines 9-14).

Turning to the *AAPA*, *AAPA* teaches in general that ohmic losses are negligible if the substrate resistivity is higher than 3 kΩ.cm (Background of the Invention at page 2, lines 16-17).

However, there is nothing about *AAPA* in combination with *Auberton-Herve* that renders the claimed method obvious at least because *Auberton-Herve* does not teach the claimed increasing charge trap density between the insulating layer and the silicon substrate.

While the Background Art may teach a general statement about ohmic losses, it is the combination of the high resistivity silicon substrate with resistivity higher than 3 kΩ.cm and the claimed increasing charge trap density between the insulating layer and the silicon substrate that renders the claimed invention patentable and thus not obvious.

Accordingly, considering the combination of *Auberton-Herve* and *AAPA* the combination does not render the claims *prima facie* obvious.

Withdrawal of the rejection of claims 20-24 and 27-31 is respectfully requested.

The rejection of claims 32-33 and 35-38 is respectfully traversed and reconsideration is requested.

Claims 32-33 and 35-38 are allowable over the cited references in that each of these claims recite a combination of elements including, for example, "a high resistivity silicon substrate with a resistivity higher than 3 kΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer, wherein the multilayer structure comprises an intermediate layer in between the high resistivity silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm, preferably smaller than 50 nm."

None of the cited references teach or suggest at least these features of the claimed invention.

In rejecting claim 32, the Examiner states, "wherein the mean size of the grains of the intermediate layer is smaller than 150nm (implicit in page 5 [0084], [0085], note: thickness of the polycrystalline layer in Fig. 1, 50 nm (page 5, [0088])(Office Action page 3)."

It is respectfully noted that *thickness of a layer is not necessarily the same as grain size*. For example, a layer may be very thick and yet contain small grains thinner than the thickness of the layer.

Furthermore, Applicant's arguments with respect to the rejection of claims 20-24 and 27-31 apply equally to the instant rejection of claims 32-33 and 35-38.

Withdrawal of the rejection of claims 32-33 and 35-38 is respectfully requested.

4. Claims 25 and 26 are rejected under 35 U.S.C. §103(a) as unpatentable over United States patent application publication 2003/0129780 A1 (*Auberton-Herve*) in view of Applicant's Admitted Prior Art (*AAPA*) and further in view of European patent application EP 1 014 452 A1 (*Inoue*).

The rejection of claims 25 and 26 is respectfully traversed. Claims 25 and 26 depend either directly or indirectly upon claim 20 and thus necessarily contain all of the limitations of claim 20.

Withdrawal of the rejection of claims 25 and 26 is respectfully requested.

5. Claim 34 is rejected under 35 U.S.C. §103(a) as unpatentable over United States patent application publication 2003/0129780 A1 (*Auberton-Herve*) in view of Applicant's Admitted Prior Art (*AAPA*) and further in view of European patent application EP 0 975 011 A1 (*Shiota*).

The rejection of claim 34 is respectfully traversed. Claim 34 depends upon claim 32 and thus necessarily contains all of the limitations of claim 32.

Withdrawal of the rejection of claim 34 is respectfully requested.

6. Prior art made of record but not relied upon in the instant rejections.

The Examiner has cited United States patent 6,368,938 B1 (*Usenko*) as art of record not relied upon but considered pertinent to Applicant's disclosure (Office Action at page 7).

Applicant notes that a similar argument as set out above for *Auberton-Herve* is applicable to *Usenko*. *Usenko* relates to a process for manufacturing a silicon-on-insulator substrate and semiconductor devices formed on such substrates. The method comprises implanting of hydrogen atoms through a face side of a wafer to a depth exceeding a depth of the silicon dioxide layer.

The implanted atoms produce numerical atom displacements which are needed to form dislocations microloops. The dislocation microloops are effective getters for heavy metals. A location of this kind of getter is advantageous for integrated semiconductor devices, as they form a layer throughout the entire wafer and at the middle of the semiconductor device layer (Col. 8 Lines 2 to 25 and Lines 51 to 60)

Again, the dislocations are formed for, preventing or overcoming contamination of the semiconductor device by metal impurities, and not for increasing charge trap density between the insulating layer and the silicon substrate. Hence, as set out above, the method of *Usenko* differs from the method according to the claimed invention.

It is thus submitted that *Usenko* in combination with the other references does not render the claimed invention obvious.

7. Conclusion.

As a result of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that every pending claim in the present application be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's attorney, the Examiner is invited to contact the undersigned at the numbers shown below.

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314-1176
Phone: (703) 683-0500
Facsimile: (703) 683-1080

Date: August 1, 2008

Respectfully submitted,

JUSTIN J. CASSELL
Attorney for Applicant
Registration No. 46,205